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EXAMINER	
FRANKLIN, RICHARD B	
ART UNIT	**PAPER NUMBER**
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,057	RAPP ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24,26-36 and 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24,26-36 and 38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
11/5/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/12/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 24, 26 – 36, and 38 are pending.

Continued Examination Under 37 CFR 1.114

2. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 12 June 2006 was filed after the mailing date of the final Office Action on 19 April 2006. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

4. Cited reference "LECURIEUX-LAFAYETTE G: "Un Seul FPGA Dope Le Traitement D'Images", Electronique, CEP Communication, Paris, FR, no. 55, 1996, pp. 98, 101-103" has not been considered by the Examiner because an English translation has not been submitted.

Response to Arguments

5. Applicant's arguments filed 25 August 2006 have been fully considered but they are not persuasive.

Applicant appears to be interpreting the relied upon reference, US Patent No. 6,308,311 (hereinafter Carmichael), differently than the Examiner. Applicant appears to be interpreting the target FPGA 10 of Carmichael to be the claimed programmable device. Applicant also appears to interpret the interface device 30 of Carmichael to be the claimed interface. However, this is not how the Examiner has interpreted Carmichael. The Examiner has interpreted the interface device 30 of Carmichael to be the programmable circuit of the claimed invention. The programmable circuit includes a programmable logic integrated circuit (Item 32), firmware memories (Items 36 and 38), and an interface to an outside device (Items 33 – 35 and 40 – 42). Target FPGA 10 and

signal lines 48 of Carmichael are not relied upon in order for Carmichael to read on the claimed invention.

As per claim 1, Applicant argues that the relied upon reference, US Patent No. 6,308,311 (hereinafter Carmichael), does not teach or suggest integration of an interface into the programmable logic integrated circuit (PLIC). Applicant continues to allege that such integration would not have been practical at the time of Carmichael (Applicant's Remarks; Page 15 Paragraph 2). An interface is a connection that allows information to pass through it. Carmichael does teach the PLIC including an interface. In Carmichael, bi-directional bus 35 and address/data bus 33 are connected to a microprocessor 34 and an FPGA 32. The connection point between the busses (Items 33 and 35) and the FPGA (Item 32) is the interface. The interface is therefore, included on the FPGA to allow information from the busses to pass into the FPGA.

As per claim 16, Applicant argues that the relied upon reference, US Patent No. 6,308,311 (hereinafter Carmichael), does not teach or suggest using the industry-standard busses as conventional busses that are connected to standard peripherals (Applicant's Remarks; Page 16 Paragraph 4). However, the claims or specification do not define what is considered to be an industry standard bus. The specification only defines an industry standard data format, such as Rapid I/O (Current Application Publication No. 2004/0170070; Paragraph [0057]). Nowhere does the specification define an industry standard bus. Therefore, any bus or wire that is used to connect to

peripherals could reasonably be considered an industry standard bus. Nowhere does Carmichael state that the USB or serial interfaces are not conventional busses that are connected to standard peripherals. In fact, Carmichael teaches that in order to use the USB interface in accordance with the Universal Serial Bus Specification Revision 1.0, a method must be followed to allow the FPGA to boot before it is detected by the host system. The claim does not limit the industry-standard bus to a structure that is limited to anything more than a single wire. Therefore, Carmichael teaches using the industry-standard busses in a standard fashion.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 2, 4 – 7, 9 – 12, 16, 20, 23, 30 – 33 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,308,311 (hereinafter Carmichael).

As per claims 1 and 30, Carmichael teaches a programmable circuit including a programmable logic integrated circuit (Figure 3 Item 32) including an interface circuit (Figure 3 [Connection between Item 32 and Items 33 and 35], See "Response to Arguments" above), the programmable logic integrated circuit operable to receive multiple versions of firmware that represents a configuration from an external source,

store the multiple versions of firmware in a memory (Figure 3 Item 36, Col 7 Lines 45 – 53), and download a selected one of the versions of firmware from the memory (Col 6 Lines 11 – 18, Col 7 Lines 58 – 60).

As per claims 2 and 31, Carmichael also teaches that the programmable circuit operates in the configuration corresponding to the downloaded version of firmware after downloading the firmware from the memory (Col 7 Lines 60 – 63).

As per claim 4, Carmichael also teaches wherein the memory comprises memory external to the programmable logic integrated circuit (Fig 3 Items 36 or 38).

As per claim 5, Carmichael also teaches a programmable circuit comprising a programmable logic integrated circuit (Figure 3 Item 32) including an interface circuit (Figure 3 [Connection between Item 32 and Items 33 and 35], See "Response to Arguments" above), the programmable logic integrated circuit operable to download from a memory storing a plurality of versions of firmware (Figure 7a Item 36) a first firmware that represents a first configuration (Col 6 Lines 22 – 35), operate in the first configuration, download from the memory a second firmware that represents a second configuration (Col 7 Lines 58 – 60), and operate in the second configuration (Col 7 Lines 40 – 65).

As per claims 6 and 11, Carmichael also teaches that the programmable logic integrated circuit is operable to receive the second firmware version from an external source while operating in the first configuration, and store the second firmware version in the memory while operating in the first configuration (Col 7 Lines 49 – 53), and wherein the second firmware version may only be received when operating in the first configuration (Col 7 Lines 45 – 53).

As per claim 7, Carmichael teaches a programmable circuit unit comprising a memory (Figure 3 Item 36), a programmable logic integrated circuit (Figure 3 Item 32) coupled to the memory, the programmable logic integrated circuit including an interface (Figure 3 [Connection between Item 32 and Items 33 and 35], See "Response to Arguments" above), the programmable logic integrated circuit can receive multiple versions of firmware that represents corresponding operating configurations of the programmable circuit from an external source (Col 6 Lines 22 – 35, Col 7 Lines 40 – 65), store the firmware in a memory (Figure 3, Col 7 Lines 49 – 53), and download the firmware from the memory (Col 7 Lines 58 – 60).

As per claim 9, Carmichael also teaches that the programmable circuit comprises a field-programmable gate array (FPGA) (Figure 3 Item 32).

As per claim 10, Carmichael teaches a programmable circuit unit comprising a memory operable to store a plurality of versions of firmware, each version respectively

representing a corresponding configurations (Figure 3 Items 36 and 38); a programmable logic integrated circuit (Figure 3 Item 32) coupled to the memory and including an interface (Figure 3 [Connection between Item 32 and Items 33 and 35], See "Response to Arguments" above); wherein the programmable logic integrated circuit is operable to download from the memory a first selected one of the versions of firmware (Col 6 Lines 27 – 35), operate in the first configuration, download from the memory a second selected one of the versions of firmware in response to the processor (Col 7 Lines 58 – 60), and operate in the second configuration (Col 7 Lines 40 – 65).

As per claim 12, Carmichael also teaches that the programmable circuit unit can load the second firmware while operating in the first configuration (Col 7 Lines 58 – 60).

As per claim 16, Carmichael teaches a computing machine comprising a processor (Figure 3 Item 20); an industry standard bus (Figure 3 Items 40 and 42) coupled to the processor, the industry standard bus adapted to be coupled to standard peripheral devices (See "Response to Arguments" above); a memory that stores a plurality of firmware configurations (Figure 3 Items 36 and 38); and a programmable logic integrated circuit (Figure 3 Item 32) coupled to the memory, and the programmable logic integrated circuit coupled to the processor through the industry standard bus, the programmable logic integrated circuit operable to receive from the processor a new firmware configuration that represents a new configuration of the programmable circuit (Col 7 Lines 40 – 44), store the new firmware configuration in the memory (Col 7 Lines

49 – 53), and download the new firmware configuration from the memory in response to the processor (Col 7 Lines 58 – 60).

As per claim 20, Carmichael teaches a computing machine (Figure 3) that includes a processor (Figure 3 Item 20); an industry standard bus coupled to the processor (Figure 3 Items 40 and 42), the industry standard bus adapted to be coupled to standard peripheral devices (See "Response to Argument" above); a memory (Figure 3 Items 36 and 38) to store a plurality of versions of firmware, each version respectively represent configurations of a programmable logic integrated circuit (Figure 3 Item 32), the programmable logic integrated circuit being coupled to the memory and being coupled to the processor through the industry standard bus (Figure 3), the programmable logic integrated circuit operable to download a selected one of the firmware versions from the memory (Col 6 Lines 27 – 35), operate in the configuration corresponding to the downloaded firmware version, download a different firmware version from the memory in response to the processor (Col 7 Lines 58 – 60), and operate in the configuration corresponding to the different firmware version (Col 7 Lines 40 – 65).

As per claim 23, Carmichael also teaches that the computing machine processor can send the selected firmware to the programmable logic integrated circuit (Col 7 Lines 40 – 44), and that the programmable-circuit can load the different firmware into the

memory in response to the processor while operating in the configuration corresponding to the selected one of the firmware versions (Col 7 Lines 49 – 53).

As per claim 32, Carmichael teaches a method comprising storing in a memory (Figure 3 Items 36 or 38) a plurality of firmware codes (Figure 7a Item 36), each firmware code representing a configuration of a programmable logic integrated circuit (Col 6 Lines 22 – 35); downloading over an industry standard bus (Figure 3 [bus between items 38 and 32a]) directly into the programmable logic integrated circuit a first firmware code that represents a first configuration (Col 6 Lines 22 – 27); operating the programmable logic integrated circuit in the first configuration (Col 6 Lines 27 – 35); downloading into the programmable logic integrated circuit second firmware that represents a second configuration (Col 7 Lines 40 – 44); and operating the programmable logic integrated circuit in the second configuration after downloading the second firmware (Col 7 Lines 40 – 65).

As per claim 33, Carmichael also teaches sending the second firmware to the programmable logic integrated circuit (Col 7 Lines 49 – 53), loading the second firmware into a memory with the programmable logic integrated circuit while the programmable logic integrated circuit is operating in the first configuration (Col 7 Lines 49 – 53), and downloading the second firmware from the memory into the programmable logic integrated circuit (Col 7 Lines 58 – 60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent Application Publication No. 2003/0061409 (hereinafter RuDusky).

As per claim 3, Carmichael teaches the programmable circuit with memory as described per claim 1 (See rejection of claim 1 above).

Carmichael does not teach that the memory is a non-volatile memory.

However, RuDusky teaches a programmable circuit that uses a non-volatile electrically erasable and programmable read-only memory (EEPROM) to store configuration information (RuDusky; Paragraph [0049]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Carmichael to include a non-volatile memory to store configuration information because doing so would allow for the configuration information to remain in the memory even with no power to the system.

As per claim 8, Carmichael teaches the programmable circuit with memory as described per claim 7 (See rejection of claim 7 above).

Carmichael does not teach that the memory is an EEPROM.

However, RuDusky teaches a programmable circuit that uses an EEPROM to store configuration information (RuDusky; Paragraph [0049]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Carmichael to include an EEPROM to store configuration information because doing so would allow for the configuration information to remain in the memory even with no power to the system.

8. Claims 13 – 15, 17 – 18, 24, 27 – 29, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent Application Publication No. 2003/0177223 (hereinafter Erickson).

As per claim 13, Carmichael teaches a programmable-circuit unit that includes a memory to hold different firmware configurations (Carmichael; Figure 3 Items 36 and 38); and a first programmable logic integrated circuit (Carmichael; Figure 3 Item 32) coupled to the memory and operable to download a first selected one of the configuration from the memory (Carmichael; Col 6 Lines 27 – 35), operate in the configuration corresponding to the first selected firmware configuration, download a first different one of the firmware configurations from the memory (Carmichael; Col 7 Lines 58 – 60), and operate in the configuration corresponding to the first different firmware configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable circuit coupled to the memory and first programmable circuit that is operable to download a second selected

firmware from the memory, operate in the second selected configuration, download a second different firmware from the memory, and operate in the second different configuration.

However, Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or field programmable gate arrays (FPGAs) (Erickson; Paragraph [0013] Lines 14 – 19) running different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include multiple FPGAs that run different versions of firmware that is updated because doing so allows firmware to be changed in a system with higher computing power than a single FPGA system.

As per claim 14, Carmichael also teaches receiving the first and second configuration from an external source while operating in the first configuration and storing the first and second configuration in the memory while operating in the first configuration (Carmichael; Col 7 Lines 49 – 53).

As per claim 15, Carmichael also teaches that the programmable logic integrated circuit is a FPGA (Carmichael; Figure 3 Item 32).

As per claim 17, Carmichael teaches the computing machine with a processor coupled to a programmable logic integrated circuit unit as described per claim 16 (See rejection of claim 16 above).

Carmichael does not teach determining whether the firmware is already stored in the memory before sending the firmware to the programmable circuit, and sending the firmware to the programmable circuit only if the firmware is not already stored in the memory.

However, Erickson teaches determining if a firmware is stored in a memory coupled to the programmable circuit (Erickson; Figure 3 Items 320 – 360) and only sending the firmware to the programmable circuit if the second firmware is not stored in the memory (Erickson; Figure 3 Item 360).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the checking to see if the firmware is already stored in the memory and not sending the firmware if it is already stored because doing so reduces the chance of sending data that has already been sent and thereby wasting processing power on a data transfer that is not needed.

As per claim 18, Erickson also teaches a configuration registry (Erickson; Figure 1 Items 130 and 140) that stores firmware (Erickson; Figure 1 Item 132, Paragraph [0014]) and indicates that the firmware represents a desired configuration (Erickson; Paragraph [0015]), and that the processor is operable to download the firmware from

the configuration registry into the programmable circuit (Erickson; Paragraph [0017] Lines 9 – 13).

As per claim 24, Carmichael teaches a computing machine comprising a processor (Carmichael; Figure 3 Item 20); an industry-standard bus (Carmichael; Figure 3 Items 40 and 42) coupled to the processor and adapted to be coupled to standard peripheral devices (See "Response to Arguments" above); a memory to hold different firmware configurations (Carmichael; Figure 3 Items 36 and 38); a first programmable logic integrated circuit (Carmichael; Figure 3 Item 32) coupled to the memory and coupled to the processor through the industry-standard bus (Carmichael; Figure 3), the first programmable logic integrated circuit operable to download a first configuration from the memory (Carmichael; Col 6 Lines 27 – 35), operate in the first configuration, download a second configuration from the memory in response to the processor (Carmichael; Col 7 Lines 58 – 60), and operate in the second configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable logic integrated circuit coupled to the memory and the first programmable circuit, and coupled to the processor through the industry standard bus, the second programmable logic integrated circuit operable to download a third firmware from the memory, operate in the third configuration, download a fourth firmware from the memory in response to the processor, and operate in the fourth configuration.

However, Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or FPGAs (Erickson; Paragraph [0013] Lines 14 – 19) running different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include multiple FPGAs that run different versions of firmware that is updated because doing so allows firmware to be changed in a system with higher computing power than a single FPGA system.

As per claim 27, Carmichael also teaches receiving the second configuration from an external source and storing it in memory while operating in the first configuration (Carmichael; Col 7 Lines 49 – 53).

As per claim 28, Erickson also teaches a separate memory unit to hold firmware information for each processor (Erickson; Figure 1 Items 120 and 122).

As per claim 29, Carmichael in combination with Erickson obviously teaches that the separate memories are disposed on separate integrated circuits because putting memories on different integrated circuits would be an obvious engineering choice (See

In re Larson, 340 F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965); *In re Wolfe*, 251 F.2d 854, 855, 116 USPQ 443, 444 (CCPA 1958)).

As per claim 34, Carmichael teaches the method as described per claim 32 (See rejection of claim 32 above) and loading the second firmware into the memory with the programmable logic integrated circuit while operating in the first configuration (Carmichael; Col 7 Lines 58 – 60) and downloading the second firmware from the memory into the programmable logic integrated circuit (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach determining if the second firmware is stored in a memory coupled to the programmable logic integrated circuit and sending the second firmware to the programmable logic integrated circuit only if the second firmware is not stored in the memory.

However, Erickson teaches determining if the second firmware is stored in a memory coupled to the programmable logic integrated circuit (Erickson; Figure 3 Items 320 – 360) and only sending the second firmware to the programmable logic integrated circuit if the second firmware is not stored in the memory (Erickson; Figure 3 Item 360).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the checking to see if the firmware is already stored in the memory and not sending the firmware if it is already stored because doing so reduces the chance of sending data

that has already been sent and thereby and wasting processing power on a data transfer that is not needed.

As per claim 36, Carmichael teaches a first programmable logic integrated circuit (Carmichael; Figure 3 Item 32) coupled to a memory that stores a plurality of firmware codes (Carmichael; Figure 3 Items 36 and 38) and operable to download a first configuration (Carmichael; Col 6 Lines 27 – 35) over an industry-standard bus (Carmichael; Figure 3 [bus between items 38 and 32a]), operate in the first configuration, download a third configuration from the memory (Carmichael; Col 7 Lines 58 – 60), and operate in the third configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable logic integrated circuit coupled to the memory and the first programmable logic integrated circuit that is operable to download a second firmware from the memory, operate in the second configuration, download a fourth firmware from the memory, and operate in the fourth configuration.

However, Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or FPGAs (Erickson; Paragraph [0013] Lines 14 – 19) running different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include multiple

FPGAs that run different versions of firmware that is updated because doing so allows for firmware to be changed in a system with higher computing power than a single FPGA system.

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent No. 6,096,091 (hereinafter Hartmann).

As per claim 19, Carmichael teaches the computing machine with a processor coupled to a programmable logic integrated circuit unit as described per claim 16 (See rejection of claim 16 above).

Carmichael does not teach that the programmable logic integrated circuit programmable circuit includes a hardwired pipeline that can operate on data.

However, Hartmann teaches the use of a reconfigurable programmable circuit unit that includes a pipeline unit (Hartmann; Figure 2, Col 2 Lines 32 – 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include a pipeline unit because doing so would speed up data processing of the system.

10. Claims 21 – 22, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent No. 6,893 873 (hereinafter Moore).

As per claim 21, Carmichael teaches the computing machine as described per claim 20 (See rejection of claim 20 above).

Carmichael does not teach that the processor has a first test port, the programmable logic integrated circuit has a second test port coupled to the first test port, and the processor is able to load the selected one of the firmware into memory via the first and second test ports.

However, Moore teaches a programmable circuit with a test port (Moore; Figures 2A – 2C Item 206). The programmable circuit performs a self-test (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and can send the result to a processor through the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the test ports and data transfer through the test ports because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

As per claim 22, Moore also teaches that the processor comprises a first test port, the programmable logic integrated circuit comprises a second test port that is coupled to the first test port (Moore; Figures 2A – 2C Item 206), the programmable logic integrated circuit can perform a self-test and send self-test data to the processor via the first and second test ports (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31), and

firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

As per claim 35, Carmichael teaches the method as described per claim 32 (See rejection of claim 32 above).

Carmichael does not teach that operating the programmable logic integrated circuit in the first configuration comprises testing the programmable logic integrated circuit, and downloading the second firmware comprises downloading the second firmware only if the programmable logic integrated circuit passes testing.

However, Moore teaches a programmable logic integrated circuit with a test port (Moore; Figures 2A – 2C Item 206). The programmable logic integrated circuit performs a self-test (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and can send the result to a processor through the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the test ports, self-test, and data transfer through the test ports only if a certain test result was discovered because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

11. Claims 26 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent Application Publication No. 2003/0177223 (hereinafter Erickson) and further in view of US Patent No. 6,893,873 (hereinafter Moore).

As per claim 26, Carmichael in combination with Erickson teaches a computing machine with multiple programmable circuits as described per claim 24 (See rejection of claim 24 above).

Carmichael in combination with Erickson does not teach the first and second programmable circuits to perform self-tests and provide the self-test data to the processor via the test ports, and then each programmable circuit loads a different firmware if the self-test data indicate a predetermined result of the self-tests.

However, Moore teaches the first and second programmable circuits to perform self-tests (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and provide the self-test data to the processor via the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67), and then each programmable circuit loads a different firmware if the self-test data indicate a predetermined result of the self-tests (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael in combination with Erickson to include the test ports, self-test, and data transfer through the test ports only if a certain test result was discovered because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

As per claim 38, Carmichael in combination with Erickson teaches a method including multiple programmable circuits as described per claim 36 (See rejection of claim 36 above).

Carmichael in combination with Erickson does not teach testing the first and second programmable circuits, and wherein loading the firmware into the programmable circuits comprises loading the firmware only if the testing indicates that the programmable circuit is functioning as desired.

However, Moore teaches testing the first and second programmable circuits (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31), and wherein loading the firmware into the programmable circuits comprises loading the firmware only if the testing indicates that the programmable circuit is functioning as desired (Moore; Figure 2c, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael in combination with Erickson to include the loading of firmware though test ports because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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